COMMERCIAL (C SUFFIX) 0 to +70°C

**LD110**
**LD111**

# LD110 LD111 3½ DIGIT A/D CONVERTER SET

August 1975

## LD110 DIGITAL A/D PROCESSOR
## LD111 ANALOG A/D PROCESSOR

## Features

- 0.05% Accuracy (Of Reading) ±1 Count
- Two Voltage Ranges—1.999 V and 199.9 mV
- Sampling Rates up to 12 Samples/Second
- FET Input for $Z_{in} > 1000\ M\Omega$
- Auto-Zero Minimizes Effects of Offset, Drift and Temperature
- Auto-Polarity
- Monolithic Bipolar—PMOS Analog Circuit
- PMOS Digital Circuit
- Multiplexed BCD Output
- Overrange and Underrange Signals Available for Auto-Ranging Capability
- TTL Compatible Outputs

## Applications

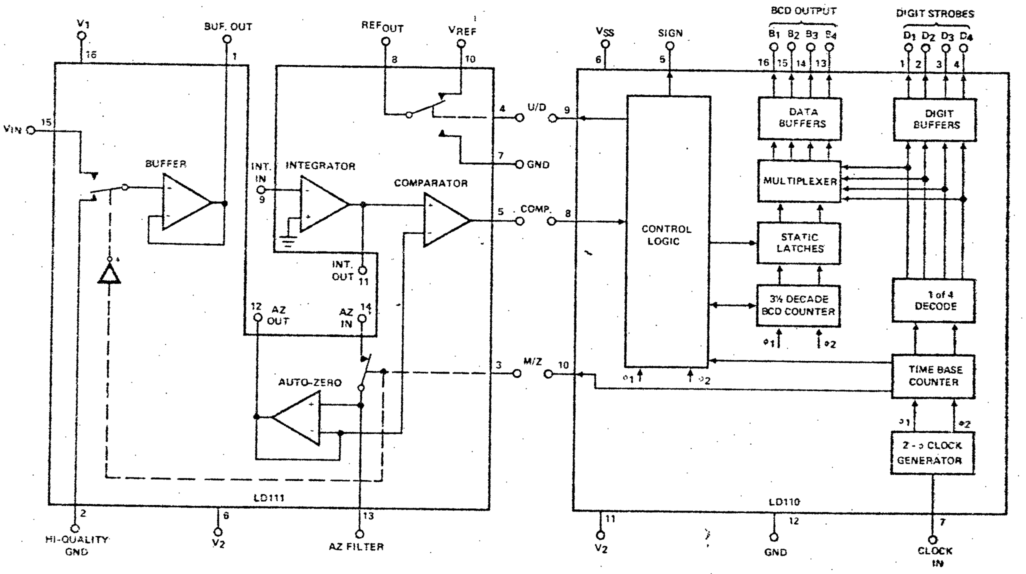
- DVM/DPM
- A/D Converters
- Controllers
- Digital Weighing Systems
- Digital Thermometers
- Process Control Instrumentation
- Scientific Instrumentation

## Description

The monolithic LD111 analog processor contains a bipolar comparator, a bipolar integrating amplifier, two MOS-FET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. A wide range of conversion rates (1/3 to 12 samples per second) as well as two voltage ranges can be accommodated using externally determined RC time constants. All amplifiers are internally compensated.

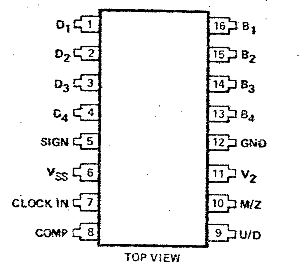
The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3½ digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2 and 4.

## FUNCTIONAL DIAGRAM



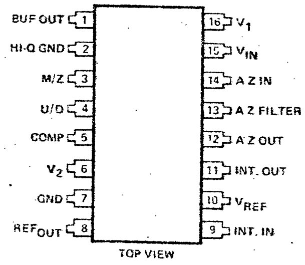
## PIN CONFIGURATIONS

**Dual-In-Line Package**



ORDER NUMBER: LD110CJ
SEE PACKAGE 8

**Dual-In-Line Package**



ORDER NUMBER: LD111CJ
SEE PACKAGE 8

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{IN}$ | ±5.0 V |
| $V_1 - V_2$ (LD111) | 30 V |
| $V_{SS}$ | 6 V |
| $V_{SS} - V_2$ (LD110) | 20 V |
| Voltage on any pin relative to $V_{SS}$ (LD110) | 0.3 V to −20 V |
| $V_{REF}$ | $V_1$ |
| Operating Temperature | 0 to 70°C |
| Storage Temperature | −65 to 150°C |
| Power Dissipation (Package)* | 750 mW |

*Device mounted with all leads welded or soldered to PC board. Derate 6.3 mW/°C above 25°C.

## ELECTRICAL CHARACTERISTICS

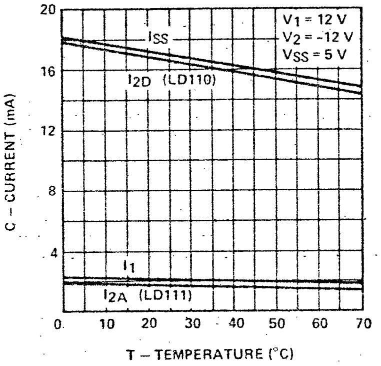
All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

| | | CHARACTERISTIC | | MIN | TYP | MAX | UNIT | TEST CONDITIONS, UNLESS NOTED: $V_1 = 12$ V, $V_2 = -12$ V, $V_{SS} = 5$ V, $V_{REF} = 8.2$ V, $T_A = 25°C$ |
|---|---|---|---|---|---|---|---|---|
| 1 | INPUT | $f_{IN}$ | Clock Frequency | | 30.7 | | KHz | 50% Duty Cycle |
| 2 | | $I_{CL}$ | Clock Input Current, Low | | | -500 | µA | $V_{CLOCK}$ in = 0.4 V |
| 3 | | $I_{IN}$ | Input Bias Current | | 4 | | pA | $T_A = 25°C$ |
| 4 | | | | | 40 | | | $T_A = 70°C$ |
| 5 | | NMR | Normal Mode Rejection | | 40 | | dB | $f_L = 60$ Hz |
| 6 | OUTPUT | $V_{OL1}$ | Measure/Zero Voltage, Low | | | 0.4 | V | $I_{OL} = 150$ µA |
| 7 | | $V_{OH1}$ | Measure/Zero Voltage, High | 2.4 | | | | $I_{OH} = -200$ µA |
| 8 | | $V_{OL2}$ | Up/Down Logic Voltage, Low | | | 0.4 | | $I_{OL} = 250$ µA |
| 9 | | $V_{OH2}$ | Up/Down Logic Voltage, High | 2.4 | | | | $I_{OH} = -200$ µA |
| 10 | | $V_{OH3}$ | Analog Comparator Voltage | 2.4 | | | | $I_{OH} = -100$ µA |
| 11 | | $V_{OL3}$ | Digits, Bits, Sign Voltage | | | 0.4 | | $I_{OL} = 1.6$ mA |
| 12 | | $V_{OH4}$ | Data Bits Voltage, High | 2.4 | | | | $I_{OH} = -200$ µA |
| 13 | | $V_{OH5}$ | Digits, Sign Voltage, High | 2.4 | | | | $I_{OH} = -800$ µA |
| 14 | SWITCH | $r_{DS(on)}$ | ON Resistance, Auto Zero Switch | | 11 | 50 | KΩ | $V_{AZ(in)} = -4.0$ V, $I_S = -50$ µA |
| 15 | | $r_{DS(on)}$ | ON Resistance, Up/Down Switch | | 650 | 3000 | Ω | $I_S = 1$ mA |
| 16 | | TC | Up/Down Switch Temperature Coefficient | | 0.20 | 0.50 | %/°C | |
| 17 | SUPPLY | $I_1$ | Supply Current | | 2.2 | 3.5 | mA | |
| 18 | | $I_{2A}$ | Supply Current, LD111 | | -1.8 | -3.0 | | |
| 19 | | $I_{2D}$ | Supply Current, LD110 | | -17 | -23 | | |
| 20 | | $I_{SS}$ | Supply Current | | 17.4 | 24 | | |
| 21 | | $PSRR_1$ | Power Supply Rejection Ratio, $V_1$ | 80 | 85 | | dB | |
| 22 | | $PSRR_2$ | Power Supply Rejection Ratio, $V_2$ | 60 | 65 | | | |
| 23 | | Reference Current Rejection Ratio | | 35 | 41 | | nA/LSB | $R_{REF} = R_2 = 100K$ Ω, $V_{IN} = 2$ V |

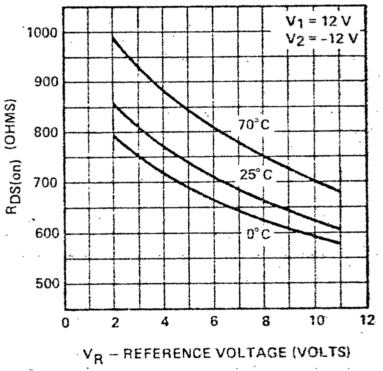
Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing. **LD110 IPAN LD111 CMAF**

## TYPICAL CHARACTERISTICS

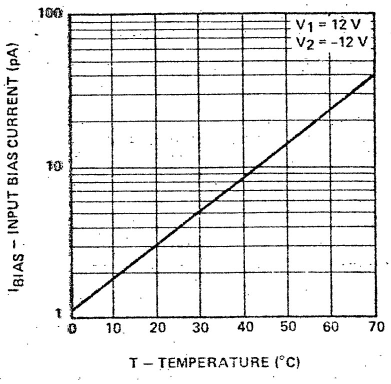
Supply Currents vs Temperature



$R_{DS(on)}$ (U/D Switch) vs $V_{REF}$ and Temperature



Input Bias Current vs Temperature



## FUNCTIONAL DESCRIPTION

The connection diagram of Figure 1 and the timing diagrams of Figures 2 and 3 will be referred to in this discussion of functional operation.

**Time Base Counter:** An external clock signal using either TTL or MOS logic levels drives a 2-$\phi$ clock generator on the synchronous digital chip. The clock frequency is divided by the time base counter into sampling intervals of 6144 pulses of which 4096 constitute the measurement interval/and 2048 the auto-zero interval. Intermediate frequency divisions are utilized by both the control logic and the 1 of 4 decoder for the digit enables and bit scan.

**Auto-Zero Interval:** The connection diagram of Figure 1 shows the analog circuitry in the auto-zero mode. The buffer amplifier input is switched to ground and supplies the relatively minor current of $V_{OS}/R_2$ to the integrator input summing node. The output of the unity gain auto-zero amplifier $V_{AZ}$ is a low-pass filtered version of the integrator output. $V_{AZ}/R_3$ and the pulsed reference Current $V_{REF}/R_1$ constitute the major currents flowing into the integrator input summing node. The reference current is pulsed at a 50% duty cycle (4 clock cycles on and 4 clock cycles off) by the control logic during this interval. The on state of the reference current corresponds with a down state of the Up/Down logic. Equilibrium will be attained by the closed loop system of integrator and AZ amplifier when the sum of the average currents at the integrator summing junction equals zero. The current through $R_3$ will then be constant at $-\frac{1}{2}\ V_{REF}/R_1$. The storage capacitor $C_{strg}$ will maintain the AZ amplifier at the AZ equilibrium voltage when the AZ switch is opened at the end of the zero interval. During the subsequent measure interval then, $V_{AZ}$ will equal $V_{strg}$.

The output of the integrator as a function of time during the auto-zero interval is shown in the timing diagram of Figure 2 along with the pertinent timing points. The beginning of this interval is characterized by a brief override period during which the 50% duty cycle of the U/D logic is inhibited while the integrator output is brought to $V_{strg}$.

**Measure Interval:** At the start of the measure interval, the Measure/Zero logic switches the analog input voltage into the input buffer amplifier. This amplifier in conjunction with $R_2$ acts as a voltage to current converter. The additional current flowing into the integrator summing node disrupts the balance achieved during the AZ interval driving the output of the integrator away from the AZ equilibrium voltage maintained as a reference by $C_{strg}$.

The comparator transmits the sense of the deviation to the control logic which attempts to re-establish the system equilibrium by using one of the two duty cycles available during the measure interval. The U/D logic is "up" one clock cycle and "down" 7 cycles for a high comparator output in the clock cycle preceding a set of 8 cycles. This will be designated duty cycle "A" as shown in Figure 3. With a low comparator output in clock cycle number 7 the U/D logic will be "up" for 7 cycles and "down" for 1 cycle in the following 8 clock cycles. This is duty cycle "B." The effect of these two reference current duty cycles on the integrator output is shown in Figure 3. It can be seen that the "up" state of the U/D logic drives the integrator output voltage up. The synchronous up/down BCD counter increments by each clock pulse when the U/D logic is "up" and decrements by each clock pulse when the U/D logic is "down." Consequently the net count goes up 6 counts for a "B" duty cycle and down 6 counts for an "A" duty cycle

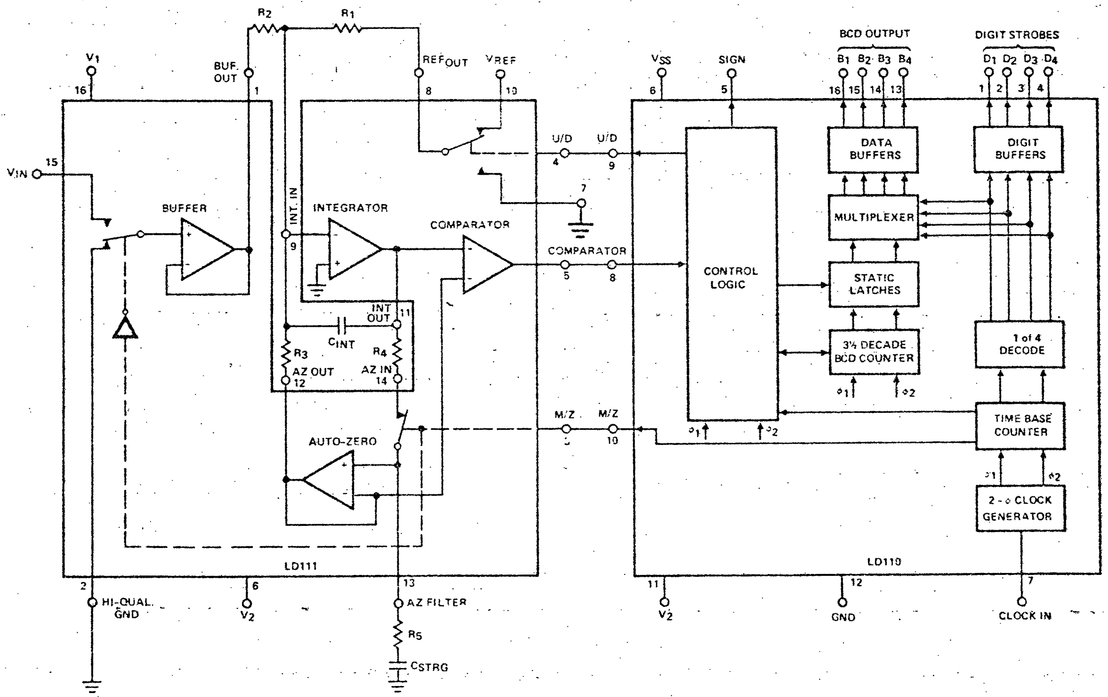


Figure 1: Connection Diagram

## FUNCTIONAL DESCRIPTION (Cont'd)

to give a maximum count of approximately 3100 counts. This counting procedure is inverted when $V_{IN} < 0$.

The polarity of $V_{IN}$ is determined by the state of the U/D logic when the BCD counter state is zero. This information, stored in the sign flip-flop, is loaded into the static latch once each measure-zero cycle.

The BCD counter accumulates a number of counts proportional to the input voltage during the measure interval as the control logic works to maintain equilibrium. Since the system equilibrium is established in steps there will exist, in all probability, a residual voltage error $\Delta V$ at the end of the measure period. This voltage and the corresponding counter error are accounted for by a brief override interval at the beginning of the auto-zero period. The counter continues its count until the integrator output $V_O$ equals the auto-zero equilibrium voltage and the U/D is "down." At this time the BCD counter is put on "hold" and its contents are loaded into the latches along with underrange information decoded from the counter contents (5% of full scale). The counter is then cleared. The contents of the static latches are multiplexed to the push-pull data output buffers in BCD format. The data output is an interlaced scan of digits 1, 3, 2 and 4 where digit 4 is the most significant digit. The presence of a count of 2000 or greater in the BCD counter (100% of full scale) causes the 3½ digit display to blink off during the zero cycle resulting in a blink rate equal to the sampling rate. All outputs are active high and TTL compatible.

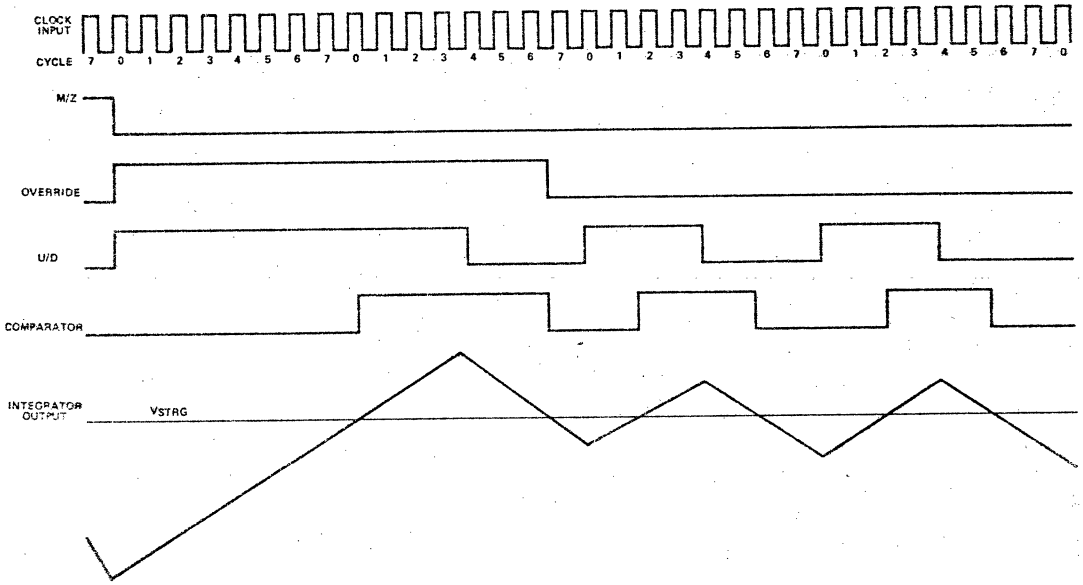

CLOCK INPUT
CYCLE 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0
M/Z
OVERRIDE
U/D
COMPARATOR
INTEGRATOR OUTPUT
VSTRG

Figure 2: Auto-Zero Timing

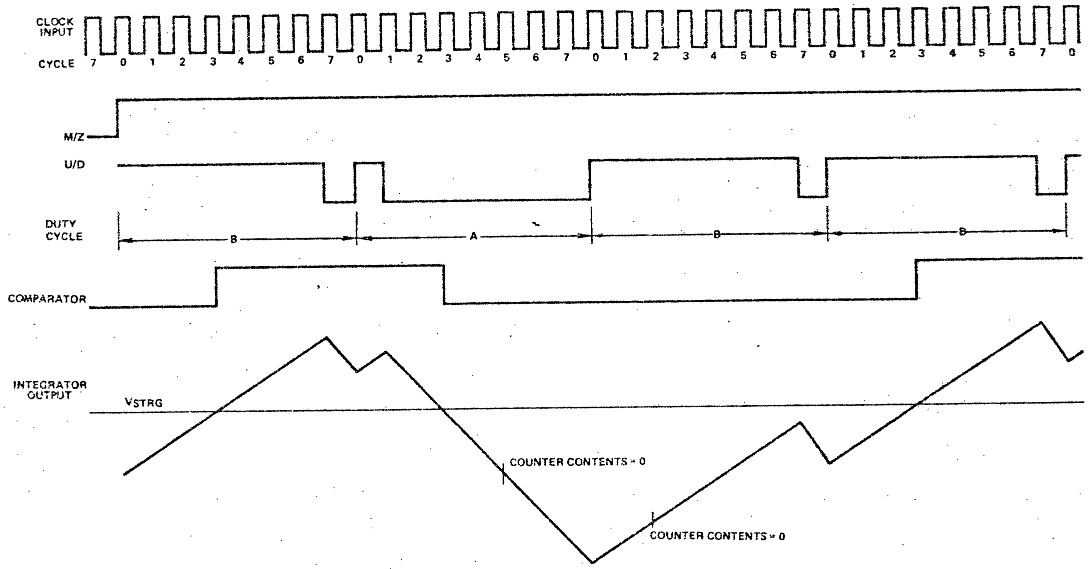


Figure 3: Measure Interval Timing

## APPLICATION INFORMATION (Refer to Application Circuit)

a) The recommended supply voltages are:

$V_1$ = 12 V ±10%
$V_2$ = −12 V ±10%
$V_{SS}$ = 5 V ±10%
$V_{REF}$ = +2.00 V to $V_1$

(Reference voltages greater than 5 volts are recommended to minimize the effects of the U/D switch ON resistance)

b) The accuracy of the A/D converter is essentially dependent on the voltage regulation of the reference voltage $V_{REF}$ as shown by the following equation:

$$V_{readout} = V_{IN} \cdot \frac{R_1'}{R_2} \cdot \frac{8.192}{V_{REF}} \pm 1 \text{ digit}$$

$R_1'$ is the sum of the reference resistance and the reference switch "on" resistance (typically 650 Ω). It can be seen that the relationship between $R_1'$, $R_2$ and $V_{REF}$ is then $V_{REF} = 8.192\ R_1'/R_2$. A trimmer resistor in series with the reference resistor will allow $R_1$ to be adjusted for the correct full scale voltage.

c) The output of the integrator $V_O$ should always be more positive than −9 volts to obtain an accurate readout for allowable input voltages.

$$V_{O(min)} > -9 \text{ V}$$

where $$V_{O(min)} = V_{strg} - \frac{7}{f_{IN}C_1}\left[\frac{V_{REF}}{2R_1} + \frac{V_{IN(max)}}{R_2}\right]$$

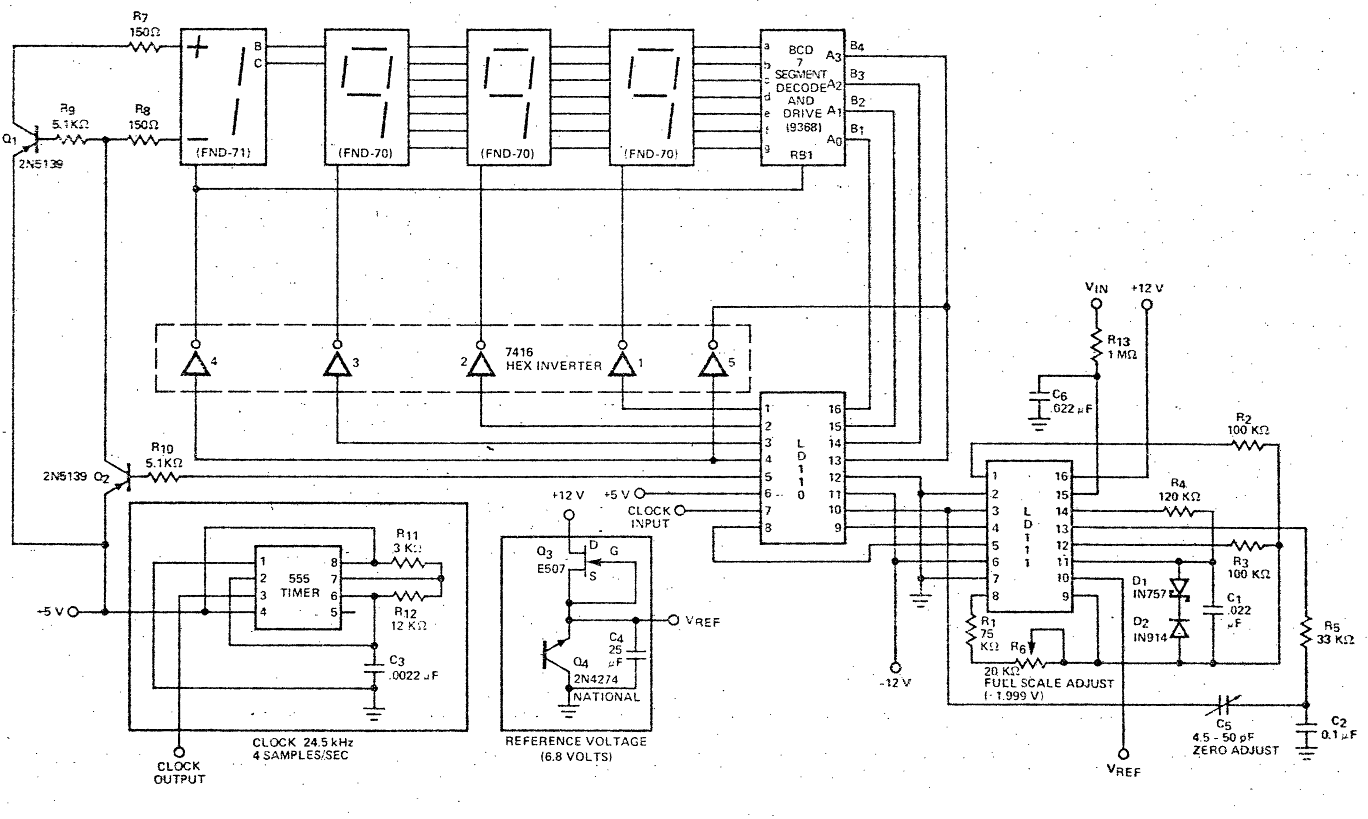
$$V_{strg} = \frac{V_{REF}\,R_3}{2R_1}$$

For any chosen reference voltage and clock frequency, $V_{strg}$, $R_1C_1$ and $R_2C_1$ should be adjusted to maintain this inequality. In addition, the product $R_2C_1f_{IN}$ should be made approximately equal to 50 to maintain the specified accuracy ($R_2C_1f_{IN}$ equals 54 for the application circuit).

A Zener diode placed in parallel with $C_1$ as shown in the application circuit will maintain the functionality of the analog processor for large positive input voltages.

d) Although any clock frequency between 2K Hz and 75K Hz may be used, clock frequencies that are integer divisions of $2048f_L$ ($f_{IN} = 2048f_L/n$, n = 2, 3, 4 . . 51, $f_L$ = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period ($T_{zero} = n/f_L$, $T_{measure} = 2n/f_L$). Line frequency interference is minimized by the selection of one of these 50 frequencies.

e) Sampling Rate = $f_{IN}/6144$



3½ Digit DVM (±2.000 Volts)

## APPLICATION INFORMATION (Cont'd)

f) The use of a 7 segment LED for digit 4 allows the DVM to be utilized up to the maximum count of 3100 (3.1 V). The output of the BCD to 7 segment decoder will be erroneous during digit 4 time however, due to overrange and underrange information encoded on bits 3 and 4 during this time. The bit 3 and 4 inputs (bit 4 being the most significant bit) of the decoder should be clamped to ground during digit 4 time to give the correct digit 4 readout—i.e.

Input C of Decoder = $B_3 \cdot \overline{D}_4$

Input D of Decoder = $B_4 \cdot \overline{D}_4$

where $B_n$ is the nth BCD data bit and $D_n$ is the nth digit.

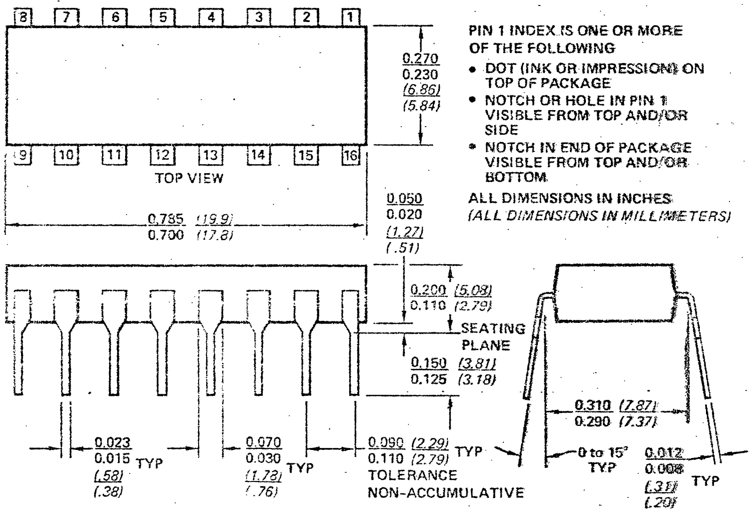
g) The overrange and underrange signals can be obtained by external logic—i.e.

MUX Underrange = $B_4 \cdot D_4$ (5% of full scale)

MUX Overrange = $\overline{D_1 + D_2 + D_3 + D_4}$ (100% of full scale)

h) Resistor $R_2$ should be 10K Ω for 200.0 mV range.

## MECHANICAL DATA



PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
*(ALL DIMENSIONS IN MILLIMETERS)*

PACKAGE 8
16 LEAD DUAL IN LINE PACKAGE (J)
(PLASTIC)

Specifications subject to change without notice.

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